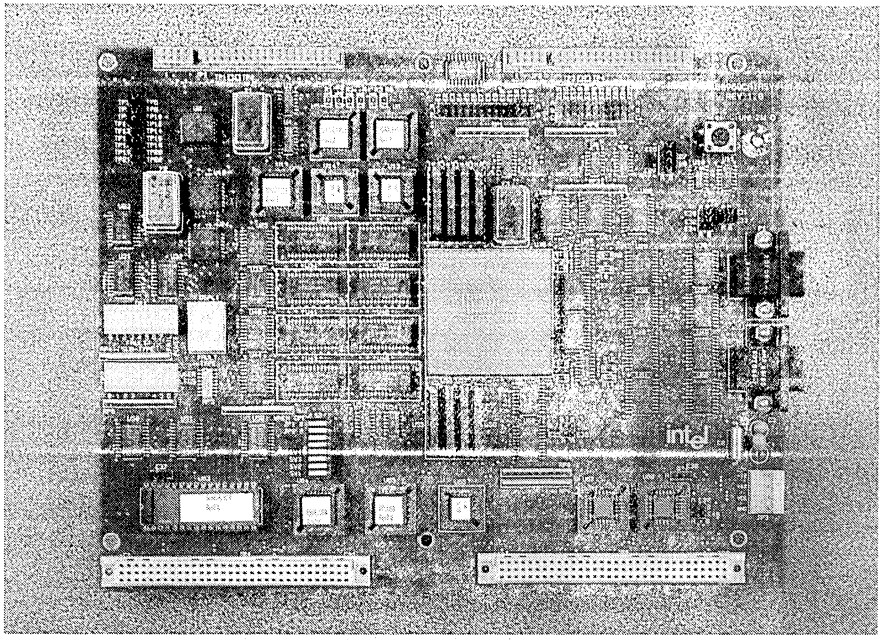
EV80960CA Evaluation Board



270870-1

Low Cost Processor Evaluation Tool

Intel's EV80960CA evaluation board provides a low-cost hardware environment for code execution and software debugging. The board features the 80960CA, the newest and highest performance member of Intel's family of 32-bit embedded microprocessors. The board allows a user's program to take full advantage of the power of the 80960CA and provides zero wait state execution of the user's code.

Popular features such as single line assembler/disassembler, single-step program execution and software breakpoints are standard on the EV80960CA's on-board monitor. Available separately, Intel offers a complete code development environment using the assembler (ASM-960) as well as high-level languages, such as Intel's iC-960 C compiler, to accelerate development schedules.

The EV80960CA evaluation board package features the 80960CA System Debug Monitor (SDM) in EPROM, a SDM host software floppy disk, a power supply cable, a 9-pin PC/AT serial connector for terminal and the EV80960CA User's Manual. The EV80960CA User's Manual includes schematics of the board, a part list and programmable logic (PLD) equations. The board is hosted on an IBM or BIOS-compatible PC/AT.

*The SRAM memory system provides zero wait state read (0-0-0-0-0) and one wait state write (1-1-1-1-0) performance.
**The DRAM memory system provides 2-1-1-1-1 reads and writes.

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EV80960CA Features

- 25 MHz Execution Speed
- 32 Kbytes of EPROM for 80960CA SDM Target Operating Firmware
- 64 Kbytes of Zero Wait State Pipelined SRAM*
- 1 Mbyte of Static-Column Mode DRAM** expandable to 4 Mbytes
- Concurrent Interrogation of Memory and Registers
- Software Breakpoints
- Code Disassembly
- High-Level Language Support
- Two RS-232s for Host and User Communication
- Two iSBX I/O Connectors
- An Expansion Bus to Accommodate Eurocard Form-Factor Prototyping Boards

Fast Pipelined SRAM Memory System

The pipelined-read memory system of the EV80960CA provides true zero wait state read and one wait state performance. The memory design utilizes the internal wait state generator of the 80960CA.

Fast Static-Column Mode DRAM

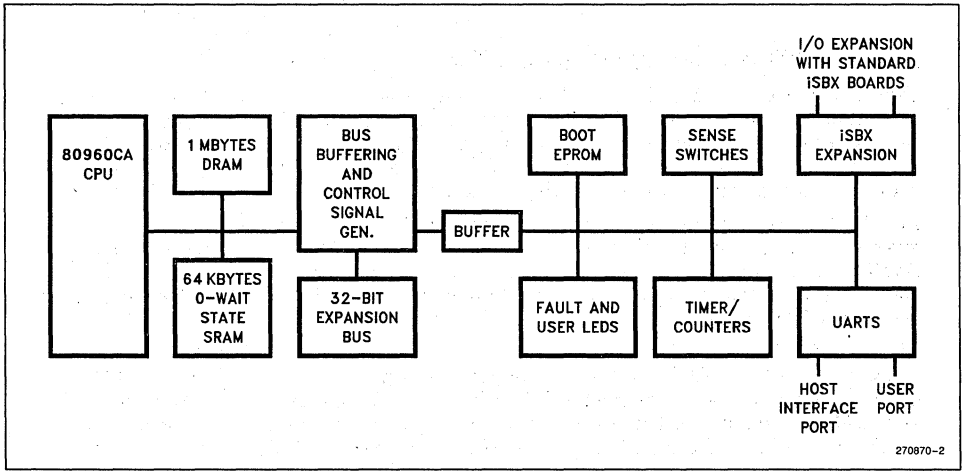
The memory design of the EV80960CA uses the 80960CA burst mode bus and static-column DRAM mode. The DRAM control PLDs are functionally isolated into interconnected state machines. The PLDs can be changed to allow alternative DRAM memory implementations with different DRAM access modes (static-column mode, nibble mode or fast-page mode).

Concurrent Interrogation of Memory and Registers

The 80960CA System Debug Monitor (SDM) for the EV80960CA allows the user to read and modify internal registers and external memory while the user's program is running on the board.

iSBX I/O Connectors and Expansion Interface

The EV80960CA evaluation board has two connectors to support both 8- and 16-bit standard iSBX Expansion Modules. The board also provides an expansion bus to accommodate Eurocard form-factor prototyping boards.



Block Diagram of the EV80960CA Board

EV80960CA Evaluation Board

Communication Link

The EV80960CA board communicates with the host through the RS-232 link using an Intel 82510 UART provided on board. The board supports seven baud rates: 300, 1200, 2400, 4800, 9600, 19200 and 38400.

Power Requirements

The EV80960CA Evaluation Board requires 5V at 2000 mA and ±12V at 25 mA.

Host System Requirements

The EV80960CA Evaluation Board is hosted on an IBM PC/AT or compatibles; a 386-based PC is recommended. The host system must meet the following minimum requirements:

- 512 Kbytes of Memory
- One 1.2 Mbyte Floppy Disk Drive
- PC-DOS 3.2 or Later
- A Serial Port (COM1 or COM2)